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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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OSHA LIANG L.L.P.
1221 MCKINNEY STREET
SUITE 2800
HOUSTON, TX 77010

EXAMINER	
PROCTOR, JASON SCOTT	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 09/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/993,074	GOMEZ ET AL.	
	Examiner	Art Unit	
	Jason Proctor	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 June 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-20 were presented for examination and rejected in Office Action dated 18 March 2005. Applicants' response has amended independent claims 1, 11, 14, and 18. Claims 1-20 have been submitted for reconsideration. Claims 1-20 have been rejected.

Priority

The Examiner thanks Applicants for identifying the inadvertent error in the previous Office Action regarding the priority date for this application. The Examiner acknowledges that this application claims priority under 35 U.S.C. § 119(e) to provisional US Application 60/252,308 filed on November 21, 2000.

Drawings

1. The drawings filed on 20 June 2005 are acceptable subject to correction of the informalities indicated on the attached "Notice of Draftsperson's Patent Drawing Review," PTO-948. In order to avoid abandonment of this application, correction is required in reply to the Office action. The correction will not be held in abeyance.

Claim Rejections – 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. § 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 1-20 are rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Amended independent claims 1, 11, 14, and 18 recite the limitation "to perform an architectural analysis of the microprocessor" which is not described by the disclosure. A search of the disclosure has revealed a single reference to an "architectural analysis" in paragraph [0025]:

> Compiler (14) handles the compiling of binaries and batch processor (16) handles the reception and processing of batch submissions. By integrating the compiling of binaries and batch processing, the system enhances the architectural analysis and debugging of microprocessor designs.

This nominal recitation of enhancing the "architectural analysis" does not adequately describe performing the analysis as recited by the claims. The claims do not recite a process of "integrating the compiling of binaries and batch processing". The act of performing an architectural analysis, in the context of the claimed method, is not described by the disclosure.

Claims 1-20 are rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Amended independent claims 1, 11, 14, and 18 recite a step of "optimizing a microprocessor design based on the architectural analysis" which is not described by the disclosure. Indeed the various descriptions of the invention in the specification, as well as the

independent claims, describe "a method of visualizing events within a microprocessor". The disclosure makes no mention of "optimizing" save for paragraph [0006], which states:

> Once the performance characteristics for a proposed design are simulated, the design can be optimized by selectively modifying the original design in view of the performance characteristics.

This nominal recitation of the act of "optimizing" is inadequate written description of what Applicants claim to have invented. The disclosure contains no description of how to "selectively modify" the original design, or upon what basis the decision to modify should be made. The cited portion of the specification is an abstract suggestion of utility and not adequate written disclosure for the claimed invention.

Claims 1-20 are further rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. In Applicants' response dated 20 June 2005, Applicants argue that:

> Read in light of the specification, an execution behavior of the instructions is some event or state following the execution of at least one instruction that can be represented in a visual and/or numerical form. (See, *e.g.*, paragraphs [0027] and [0029] of the Instant Specification).

This argument was provided in an attempt to clearly define the phrase "an execution behavior of the instructions", however this definition is not supported by the specification at paragraphs [0027], [0029], or elsewhere. In contrast, paragraph [0029] states that the present invention "may use an external simulator to obtain the internal state information to display an execution behavior of a set of instructions." None of the independent claims explicitly require an external simulator. Applicants have failed to show where the written description supports a "numerical

form" of "an execution behavior of the instructions". The Examiner is also confused by Applicants' argument in that the argument implies that the execution of some instructions do not result in "an execution behavior" (compare "**an** event or state" to "**some** event or state"). The written description contains no explanation of when "an execution behavior of the instructions" occurs. In light of Applicants' arguments, it is apparent that Applicants regard the claimed invention as different from or possessing features absent from the written description of the application, necessitating this rejection.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-20 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the term "an execution behavior of the instructions" which renders the claim vague and indefinite. A person of ordinary skill in the art would recognize several different interpretations of this term. "Execution behavior" could comprise memory usage, memory page faults, instruction prefetching, interrupt requests, cooperative scheduling, use of particular instructions, CPU usage, and many other concepts. As a result, the claim is vague and indefinite because there is no indication what interpretation should be given to the term "execution behavior".

Independent claims 11, 14, and 18 are similarly vague and indefinite for their use of the term "execution behavior". Where dependent claims recite "execution behavior", they are similarly vague and indefinite.

Claims not specifically mentioned stand rejected by virtue of their dependency.

In response to this rejection, Applicants argue primarily that:

> Applicant respectfully acknowledges it would be clear to one skilled in the art that the term "an execution behavior of the instructions" may include, among other things, the list of concepts asserted by the Examiner. [...] Read in light of the specification, an execution behavior of the instructions is some event or state following the execution of at least one instruction that can be represented in a visual and/or numerical form. (See, *e.g.*, paragraphs [0027] and [0029] of the Instant Specification).

The Examiner has reviewed the entire disclosure as well as the cited portions of the specification (paragraphs [0027] and [0029]) but fails to find adequate support for Applicants' argument. These paragraphs appear to be directed toward displaying selectable buttons and using an external microprocessor simulator. The Examiner notes that paragraph [0022] states:

> The present invention is a user-friendly tool that aids in the analysis of microprocessor performance characteristics. The present invention addresses the visualization of microprocessor internal resource utilization and correlation to instruction flow for the purpose of performance analysis and functional verification.

However, this teaching is not described as specifically related to "an execution behavior of the instructions". As stated previously, there is no indication what interpretation should be given to the term "execution behavior". Applicants' arguments have been fully considered, but have been found unpersuasive.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1-20 are rejected under 35 U.S.C. § 103(a) as being unpatentable over US Patent No. 6,209,126 to Sasaki et al. (Sasaki) in view of US Patent No. 6,490,716 to Gupta et al. (Gupta).

Regarding claim 1, Sasaki discloses a technique of analyzing the pipeline processing of a source program to be executed in a microprocessor wherein an instruction developing unit develops each instruction line of the interpreted source program into states in pipeline stages of the pipeline processing (column 3, lines 47-50) and the image creator creates a pipeline image information that indicates the states of the instructions contained in the source program in pipeline stages (column 4, lines 3-5). The image display controller displays the source program and the pipeline image (column 4, lines 6-10; see also Figs. 6-16).

Sasaki discloses performing an optimization of the source program but does not explicitly disclose performing an optimization of the microprocessor.

Gupta teaches that it is known in the art to optimize a microprocessor designed for a specific task (column 1, lines 44-61). In this case, it would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to combine the teachings of Gupta with the technique disclosed by Sasaki to achieve a method wherein the pipeline image information is used to optimize a microprocessor design. Motivation to do so could be found explicitly in Gupta or in the nature of the problem to be solved, such as in the circumstance where the source program cannot be altered for whatever reason but the microprocessor is still under design.

Regarding claim 2, Sasaki discloses analyzing a source program (set of instructions) according to an execution history (executing the set of instructions) with regard to stalls in the pipeline processing of the program (column 4, lines 38-58). Sasaki gives an exemplary suggestion that the execution history be provided by a simulator, however it is inherent that a simulator of a microprocessor performs equivalently to the microprocessor being simulated.

Regarding claim 3, Sasaki discloses simulating the execution of a set of instructions and generating internal state information representative of events occurring in the microprocessor from the simulation (column 4, lines 38-58).

Regarding claim 4, Sasaki discloses simulating the execution of a set of instructions and generating internal state information representative of events occurring in the microprocessor

from the simulation (column 4, lines 38-58). It is inherent that the simulator receives the set of instructions; therefore the instructions are exported to the simulator.

Regarding claim 5, Sasaki discloses displaying a number of instructions (Figs. 6-16; instructions such as "NOP" and "ADD" depicted on the left portion of the display; column 4, lines 31-37).

Regarding claim 6, Sasaki discloses displaying instructions occurring during a selected number of time periods (Figs. 6-16; numbered rows of the display correspond to instructions, equivalently clock steps).

Regarding claim 7, Sasaki discloses reading a history of simulated execution, equivalent to a log (column 4, lines 45-60).

Regarding claim 8, Sasaki discloses displaying instructions, simulating operation of the instructions, and generating internal state information representative of events occurring in the microprocessor (column 4, lines 31-60).

Regarding claim 9, Sasaki discloses displaying the internal state information (Figs. 6-16; column 4, lines 3-10). It is inherent that the system taught by Sasaki converts data as necessary in order to produce the graphical display.

Regarding claim 10, Sasaki discloses displaying the flow of instructions through a pipeline (Figs. 6-16; column 3, lines 47-55; column 4, lines 3-10).

Claims 11-20 generally recite a software tool, system, or tool that implements a method comprising various combinations of the limitations of claims 1-10, as indicated below. As the Sasaki in view of Gupta teaches all of the limitations as recited by claims 1-10, so does Sasaki in view of Gupta teach those limitations in other combinations.

Claims 11-13 recite a software tool that implements the methods of claims 1-3. As Sasaki in view of Gupta teaches a computer-implemented technique (abstract), claims 11-13 are rejected for the same reasons as those given above for claims 1-3.

Claim 14 recites a system that implements the methods according to the combined limitations of claims 1 and 4. Claims 15-17 recite further limitations that correspond to claims 5, 6, and 9, respectively. As Sasaki in view of Gupta teaches a computer-implemented system (abstract), claims 14-17 are rejected for the same reasons as those given above for claims 1, 4-6, and 9.

Claim 18 recites a tool that implements the method of claim 1. Claim 19 recites a tool that implements the method of claim 3. Claim 20 recites a tool that implements the method of claims 4 and 9. As Sasaki in view of Gupta teaches a computer-implemented technique (abstract), claims 18-20 are rejected for the same reasons given above for claims 1, 3, 4, and 9.

Conclusion

Art considered pertinent by the examiner but not applied has been cited on form PTO-892.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Proctor whose telephone number is (571) 272-3713. The examiner can normally be reached on 8:30 am-4:30 pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Picard can be reached at (571) 272-3749. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jason Proctor
Examiner
Art Unit 2123

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Paul L. Rodriguez 8/25/05
Primary Examiner
Art Unit 2125